	Type	L #	Hits	Search Text	DBs
1	BRS	L1	741	multiple same level same cach$	USPAT
2	BRS	L2	803	l1 same cache	USPAT
3	BRS	L3	1185	l2 same cache	USPAT
4	BRS	L4	166	monitor$ same cache same activity	USPAT
5	BRS	L5	35	high same level same load same queue	USPAT
6	BRS	L6	339	reload same buffer$1	USPAT
7	BRS	L7	4221	register same load same bus	USPAT
8	BRS	L8	1052	cache same load same bus	USPAT
9	BRS	L9	225	1 and 2	USPAT
10	BRS	L10	204	9 and 3	USPAT
11	BRS	L11	6	4 and 10	USPAT
12	BRS	L12	0	11 and 5	USPAT
13	BRS	L13	0	11 and 6	USPAT
14	BRS	L14	76	6 and 7	USPAT
15	BRS	L15	43	8 and 14	USPAT
16	BRS	L16	6	2 and 15	USPAT
17	BRS	L17	5	3 and 16	USPAT

	Time Stamp	Comments	Error Definition	Errors
1	2000/12/15 18:59			0
2	2000/12/15 18:59			0
3	2000/12/15 18:59			0
4	2000/12/15 19:00			0
5	2000/12/15 19:00			0
6	2000/12/15 19:00			0
7	2000/12/15 19:01			0
8	2000/12/15 19:01			0
9	2000/12/15 19:01			0
10	2000/12/15 19:01			0
11	2000/12/15 19:01			0
12	2000/12/15 19:01			0
13	2000/12/15 19:02			0
14	2000/12/15 19:02			0
15	2000/12/15 19:02			0
16	2000/12/15 19:02			0
17	2000/12/15 19:02			0

Most Frequently Occurring Classifications of Patents Returned
From A Search of 09340074 on November 08, 2000

Combined Classifications

17 711/118 (2 OR, 15 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching

12 711/144 (3 OR, 9 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency
711/144 ....Cache status data bit

12 712/215 (2 OR, 10 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/214 INSTRUCTION ISSUING
712/215 .Simultaneous issuance of multiple instructions

12 712/23 (1 OR, 11 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE
712/23 .Superscalar

11 711/122 (4 OR, 7 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/119 ...Multiple caches
711/122 ....Hierarchical caches

10 711/141 (5 OR, 5 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency

9 711/119 (2 OR, 7 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/119 ...Multiple caches

9 711/145 (0 OR, 9 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency
711/145 ....Access control bit

8 711/146 (2 OR, 6 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency
711/146 ....Snooping

7 711/143 (2 OR, 5 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency
711/143 ....Write-back

7 712/210 (4 OR, 3 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING

SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING

712/209 .Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.)

712/210 .Decoding instruction to accommodate variable length instruction or operand

7 712/218 (5 OR, 2 XR)

Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING

712/216 DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING OR CONFLICT RESOLUTION

712/218 .Commitment control or register bypass

5 711/128 (4 OR, 1 XR)

Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

711/100 STORAGE ACCESSING AND CONTROL

711/117 .Hierarchical memories

711/118 ..Caching

711/128 ...Associative

5 711/133 (3 OR, 2 XR)

Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

711/100 STORAGE ACCESSING AND CONTROL

711/117 .Hierarchical memories

711/118 ..Caching

711/133 ...Entry replacement strategy

5 711/137 (0 OR, 5 XR)

Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

711/100 STORAGE ACCESSING AND CONTROL

711/117 .Hierarchical memories

711/118 ..Caching

711/137 ...Look-ahead

5 711/147 (0 OR, 5 XR)

Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

711/100 STORAGE ACCESSING AND CONTROL

711/147 .Shared memory area

5 711/202 (2 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/202 .Address mapping (e.g., conversion, translation)

5 712/200 (0 OR, 5 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/200 ARCHITECTURE BASED INSTRUCTION PROCESSING

5 712/207 (0 OR, 5 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/205 INSTRUCTION FETCHING
712/207 .Prefetching

5 712/213 (2 OR, 3 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/209 .Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.)
712/213 .Predecoding of instruction component

5 712/228 (2 OR, 3 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/228 .Context preserving (e.g., context swapping, checkpointing, register windowing

4 711/131 (2 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/131 ...Multiport cache

4 711/213 (3 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/213 .Generating prefetch, look-ahead, jump, or predictive address

4 711/3 (0 OR, 4 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/1 ADDRESSING COMBINED WITH SPECIFIC MEMORY CONFIGURATION OR SYSTEM
711/3 .Addressing cache memories

4 712/204 (3 OR, 1 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/204 INSTRUCTION ALIGNMENT

3 709/108 (1 OR, 2 XR)
Class 709 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MULTIPLE COMPUTER OR PROCESS COORDINATING
709/100 TASK MANAGEMENT OR CONTROL
709/102 .Process scheduling
709/107 ..Multitasking, time sharing
709/108 ...Context switching

3 711/113 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/101 .Specific memory composition
711/111 ..Accessing dynamic storage device
711/112 ...Direct access storage device (DASD)
711/113 ....Caching

3 711/117 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories

3 711/123 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING

SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/119 ...Multiple caches
711/123 ....User data cache and instruction data cache

3 711/124 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/119 ...Multiple caches
711/124 ....Cross-interrogating

3 711/129 (2 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/129 ...Partitioned cache

3 711/130 (1 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/130 ...Shared cache

3 711/138 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/138 ...Cache bypassing

3 711/171 (2 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL

711/170 .Memory configuring
711/171 ..Based on data size

3 711/201 (1 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/201 .Slip control, misaligning, boundary alignment

3 711/204 (0 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/202 .Address mapping (e.g., conversion, translation)
711/203 ..Virtual addressing
711/204 ...Predicting, look-ahead

3 712/217 (0 OR, 3 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/216 DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING OR CONFLICT RESOLUTION
712/217 .Scoreboarding, reservation station, or aliasing

3 712/24 (2 OR, 1 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE
712/24 .Long instruction word

3 712/34 (1 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE
712/32 .Microprocessor or multichip or multimodule processor having sequential program control
712/34 ..Including coprocessor

2 345/501 (1 OR, 1 XR)

Class 345 : COMPUTER GRAPHICS PROCESSING, OPERATOR INTERFACE PROCESSING, AND SELECTIVE VISUAL DISPLAY SYSTEMS
345/501 COMPUTER GRAPHIC PROCESSING SYSTEM

2 345/520 (1 OR, 1 XR)
Class 345 : COMPUTER GRAPHICS PROCESSING, OPERATOR INTERFACE PROCESSING, AND SELECTIVE VISUAL DISPLAY SYSTEMS
345/501 COMPUTER GRAPHIC PROCESSING SYSTEM
345/520 .Interface (e.g., controller)

2 710/260 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/260 INTERRUPT PROCESSING

2 711/120 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/119 ...Multiple caches
711/120 ....Parallel caches

2 711/139 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/138 ...Cache bypassing
711/139 ....No-cache flags

2 711/140 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/140 ...Cache pipelining

2 711/150 (1 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING

SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/147 .Shared memory area
711/150 ..Simultaneous access regulation

2 711/154 (1 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/154 .Control technique

2 711/155 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/154 .Control technique
711/155 ..Read-modify-write (RMW)

2 711/158 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/154 .Control technique
711/158 ..Prioritizing

2 711/168 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/167 .Access timing
711/168 ..Concurrent accessing

2 711/206 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/202 .Address mapping (e.g., conversion, translation)
711/203 ..Virtual addressing
711/206 ...Translation tables (e.g., segment and page table or map)

2 711/207 (1 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

711/200 ADDRESS FORMATION
711/202 .Address mapping (e.g., conversion, translation)
711/203 ..Virtual addressing
711/206 ...Translation tables (e.g., segment and page table or map)
711/207 ....Directory tables (e.g., DLAT, TLB)

2 711/210 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/200 ADDRESS FORMATION
711/202 .Address mapping (e.g., conversion, translation)
711/210 ..Resolving conflict, coherency, or synonym problem

2 712/205 (2 OR, 0 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/205 INSTRUCTION FETCHING

2 712/206 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/205 INSTRUCTION FETCHING
712/206 .Of multiple instructions simultaneously

2 712/208 (1 OR, 1 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/208 INSTRUCTION DECODING (E.G., BY MICROINSTRUCTION, START ADDRESS GENERATOR, HARDWIRED)

2 712/212 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/209 .Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.)
712/212 .Decoding by plural parallel decoders

2 712/216 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/216 DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING OR CONFLICT RESOLUTION

2 712/234 (1 OR, 1 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
712/234 ..Conditional branching

2 712/237 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
712/234 ..Conditional branching
712/237 ...Prefetching a branch target (i.e., look ahead)

2 712/239 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
712/234 ..Conditional branching
712/239 ...Branch prediction

2 712/240 (2 OR, 0 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
712/234 ..Conditional branching

712/239 ...Branch prediction
712/240 ....History table

2 712/244 (2 OR, 0 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
712/244 ..Exeception processing (e.g., interrupts and traps)

2 712/245 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/220 PROCESSING CONTROL
712/245 .Processing sequence control (i.e., microsequencing)

2 712/42 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE
712/32 .Microprocessor or multichip or multimodule processor having sequential program control
712/42 ..Operation

2 712/6 (1 OR, 1 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE
712/2 .Vector processor
712/6 ..Controlling access to external vector data

2 714/2 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/2 ..Fault recovery

2 714/35 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/25 ..Fault locating (i.e., diagnosis or testing)

714/32 ...Particular stimulus creation
714/35 ....Substituted or added instruction (e.g., code instrumenting, breakpoint instruction)

2 714/710 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/710 .Replacement of memory spare location, portion, or segment

2 714/8 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/2 ..Fault recovery
714/3 ...By masking or reconfiguration
714/5 ....Of memory or peripheral subsystem
714/8 .....Isolating failed storage location (e.g., sector remapping)